PROPOSED THERMAL MODEL OF SILICON-ON-INSULATOR (SOI) INTEGRATED CIRCUITS

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Abstract: The Silicon-on-insulator (SOI) metal oxide semiconductor field effect transistor (MOSFET) structure with a layer of buried silicon oxide added to isolate the device body and the silicon substrate can significantly cut down source and drain depletion capacitances and can reduce the effect of short channel. Though, the low thermal conductivity of the buried oxide (BOX) can cause local heating, changed electrical properties, altered heat flow down interconnects, and failure of thermal devices. The current thermal models that are presently used in simulation of a circuit account for thermal effects do not accurately capture the heat flow in the devices. However, accurate models rely on large network circuits or arithmetic simulations which does not execute speedily enough for large scale integrated circuit (LSIC) simulation. The drive of this research work is to advance a method that is efficient balance between accuracy, adaptability and speed and can be used in large scale simulation. The approach will integrate efficient SOI device thermal model and communicate thermal model into integrated circuit (IC) simulation, and will offer accurate, effective and efficient electro-thermal simulation tool for large scale SOI integrated circuit structure.

Keywords: Thermal model, silicon-on-insulator (SOI), integrated circuits

Introduction

Due to advancement of technology, the demand for faster and cheaper microelectronic devices has led to a serious reduction of devices and a corresponding intensification in module density. This current technology comes with it challenging problems of heat transfer. Thermal power is produced at several device junctions, and the heat needs to diffuse away from the components, or the devices would suffer from self-heating heating effects, including degradation of reliability and effective electronic performance. Some of these junctions include considerable power dissipation. The oxide of SOI structure has a low thermal conductivity of about 1.4 W/m/K, which may be equated with values near 100 W/m/K in bulk silicon (Cheng et al., 2004). Due to the fact that the oxide is buried between the silicon device body and silicon substrate, self-heating in such SOI structure is significantly enhanced. It was estimated that the average rate of failure in semiconductor devices multiply for every 10K increase in temperature (Lin et al., 2004). The component self-heating in a device give rise to increases in the device temperature which improve impact ionization rate, it also increases the losses due to leakage current at junctions, and more also decreases movement due to stronger scattering, and then alter the electrical features of SOI device (Yu & Cheng, 2004). Additionally, the component self-heating improves heat flow from devices to interconnects, and raises metal-line and chip temperatures, which can lead to strong electro-migration in interconnects (Bar-Cohen & Avram, 2000). Increase in temperature in microelectronic devices and interconnects should be cautiously modeled to regulate the effects on the mechanical and electrical parameters and reliability of devices and interconnects.

Thermal Models in Silicon-on-insulator (SOI) Structures

(a) Conventional approaches

The analysis of thermal in semiconductor devices or interconnects are based on the heat flow given by the equation.

\[ \rho c \frac{\partial T}{\partial t} - \nabla \cdot (k \nabla T) = p_d, \]  

where, \( k \) is the thermal conductivity, \( \rho \) is density, \( C \) is specific heat, and \( p_d \) is power density. The SOI MOSFET structure shown in Figure 1, because most of potential change appears (i.e., most of power/heat is generated) near the channel-drain junction, \( p_d \) can be approximated by

\[ p_d = \frac{V_{ds} I_d}{I_{SI} W} \delta(x - x_j), \]

where \( V_{ds} \) is the drain-to-source voltage, \( I_d \) is the drain current, \( W \) is the width of device, \( I_{SI} \) is the silicon island thickness, and \( x_j \) is the location of the channel-drain junction. For boundary conditions, the heat flow into the air is neglected, and heat transfer to the oxide on top of the device in Figure 1 is also assumed to be negligible (Cheng et al., 2004). If the length of field oxide (FOX), \( L_{FOX} \), is large enough (greater than the thermal length in FOX), it can be further assumed that the heat transfer sidewise is also negligible. These assumptions can also be expressed by the adiabatic conditions \( \frac{\partial T}{\partial \lambda} = 0 \), where \( \lambda \) is the outward derivative around the surfaces dotted in Fig. 1. Due to the large thermal conductivity, the temperature of the silicon substrate is taken to be 300K. In the lightly doped substrate, thermal conductivity \( k_{sub} \approx 148W / Km \), in the thin silicon island, \( k_{SI} \approx 63W / Km \), and in the oxide, \( k_{ox} \approx 1.4W / Km \) (Peck, 1971). Instead of using numerical methods, heat flow in devices based on Cheng et al. (2004), can essentially be simulated.
Table 1: Analogy between electric and thermal circuits

| Charge, Q [C] | Energy, W [J] |
| Voltage, V [V] | Temperature, T [K] |
| Current, I [A] = (C/s) | Power, p [W]= [J/s] |
| Charge flux, J = -σV [A/m²] | Heat flux, H = -kV [W/m²] |
| Conductivity, \( \sigma \) [A/Vm] | Thermal conductivity, \( k \) [W/Km] |
| Capacitance, \( C \) [F]= [C/V] | Thermal capacitance, \( C_a \) [J/C°C] |
| Resistance, \( R = V / I \) | Thermal resistance, \( R_{th} = T / p \) [V/A] |
| Conductance, \( G = I / V \) | Thermal conductance, \( G_{th} = P / T \) [A/V] |
Thermal Model of Silicon-on-Insulator

Table 2: Summary of the short-channel interconnect model (Peck, 1971)

\[
\frac{\partial^2 T_{Si}}{\partial x^2} = \frac{T_{Si}}{Z_{Si,n}} + \frac{T_{Si} - T_{int,n}}{Z_{Si, int,n}} = \frac{T_{Si} - T_{eff,n}}{Z_{eff,n}},
\]

(5)

\[Z_{Si,n} = R_{thf} k_{Si,n} L_{thf,n} w_{Si},\]
\[Z_{Si, int,n} = R_{thf} k_{Si, int,n} A_{Si, int,n} t_{Si},\]
\[T_{eff,n} = \left(\frac{Z_{Si,n}}{Z_{Si,n} + Z_{Si, int,n}}\right) T_{int,n}.
\]

\[T_{Si}\] is the temperature in the silicon film
\[T_{int,n}\] is the temperature at the end of a poly or metal line that extends into region n
\[R_{thf}\] is the thermal resistance of the interconnect that extends into region n
\[R_{thf}\] is the film thermal resistance that describe heat flow from the film to the substrate
\[k_{Si, n}\] is the thermal conductivity of silicon in region n
\[t_{Si}\] is the thickness of the silicon film
\[w\] is the width of the device
\[L_{thf,n}\] is the length of region n in the silicon film

It was noted that the film thermal resistant \(R_{thf}\) is defined differently from \(R_{thf}\) given in equation 3. \(R_{thf}\) is defined as (Peck, 1971)

\[R_{thf} = \left(\frac{T_{Si}}{P}\right) = t_{box} k_{box, eff} A_{Si} = \frac{t_{box}}{k_{box, eff} w L_{Si}}.
\]

where \((T_{Si})\) is the average temperature along the silicon thin film, \(k_{box, eff}\) is the effective BOX thermal conductivity accounting for heat flow from the silicon film through BOX/FOX to the substrate, and \(A_{Si}\) and \(L_{Si}\) are the silicon film area and length, respectively.

Equation 5 can then be solved using proper boundary conditions following Peck (1971); Blaauw et al. (2003). Most simplified cases yield logical models in terms of infinite series. For other cases, we transform equation 5 into the general matrix equation into the more general tri-diagonal matrix equation as;

\[P = G_{th}, T,
\]

which is a generalization of the last line of Table 1, and solve this model instead. The \(G_{th}\) factor here accounts for thermal conductance for transverse and longitudinal heat flow in the silicon thin island, BOX/FOX and the interconnects.

For long interconnects with respect to the characteristic thermal length \(\lambda_{int}\) of the interconnect lines, a long interconnect approach is needed instead. Table 3 shows the derivation of \(\lambda_{int}\).

Table 3 Characteristic length, \(\lambda_{int}\)

\[\lambda_{int}^2 = \frac{k_{int}}{k_{ox, eff}} (t_{ox} t_{int})
\]

(8)

\[k_{ox, eff} \approx \left(\frac{k_{ox} h}{0.15 w}\right) \left(\frac{k_{int} t}{k_{ox} w}\right)^{0.1} \ln\left[1 + \frac{h}{w}\right]^{0.66}
\]

(9)

\(k_{ox}\) is the thermal conductivity of the interconnects or poly lines
\(k_{ox}\) is the thermal conductivity of the oxide
\(h, w, t\) are the height, width, and thickness of the rectangular interconnects, respectively

In this circumstance, interconnects may not be modeled as simple thermal resistors because the heat flow from the interconnect/poly lines to the surrounding oxide may not be neglected. Instead, they must be represented as exponential functions as in (Blaauw et al., 2003). Though, after satisfying appropriate boundary conditions, it is found that the tri-diagonal matrix equation 7 is recovered with the matrix and vector elements accounting for additional heat flow from the interconnect/poly lines to oxide, and the same form of the equation may be used. It can be shown that, with \(\lambda_{int} >> L_{ox}\), the long-interconnect approach reduces to the short-interconnect approximation.

**Proposed Work**

Numerous problems still continue with the thermal model presented above (Peck, 1971 & Blaauw et al., 2003). One of the items is that the \(G_{th}\) elements that describe the devices themselves are intermixed with the elements that describe interconnects. This is extremely undesirable for large-scale ICs simulation because \(G_{th}\) is dependent on the interconnect layout. Each time the user would input a new IC structure, and new matrix elements would need to be constructed. For the
simple current mirror in Blaauw et al. (2003), this is acceptable, but the problem becomes higher as the number of elements increases. Additionally, the joule heat in the interconnect metal lines is not considered in the model described in Section 2, which is practicable for a small circuit, such as the current mirror structure in Blaauw et al. (2003) where the two (2) SOI devices are placed in close to nearness. For IC structure with long or high density interconnect lines, joule heat induced in the metal lines must be included to predict more accurate temperature distributions.

Conclusion
The objective of the research is to rationalize the model so that it can be implemented on a larger scale. The device and interconnect matrix equations describing the heat flow in devices and interconnects, respectively, need to be separated so that a user can modify elements in the interconnect matrices/vectors without change any element in the device matrices/vectors. Interface temperatures between devices and interconnects have to be appropriately allocated and evaluated to adequately handle the heat flow between interconnects and devices. The joule heating in interconnects will be implemented in the interconnect matrices and vectors. A user interface simplifying the entry of interconnect matrix/vector elements based on the IC layouts may be designed. The research work aim at developing algorithm to assign the interconnect matrix elements automatically based VLS layouts. More also, the research work create a concept and proof of system illustrating that the steady state model functions on a large scale. The developed model for the SOI IC is expected to be coupled alongside the SPICE circuit simulator to carry out the electro-thermal simulation. The developed model will be compared to 3D commercial device and interconnect simulators to demonstrate the validity and efficiency of the model. When the model is properly implemented, it is expected that it will give an efficient tool for accurate thermal simulation in SOI devices and contribute to the development of SOI-based circuits.

Conflict of Interest
Authors declare that there are no conflicts of interest.

References